Remarks

Office Action dated May 18, 2005, rejects all claims as anticipated by the US Pat. No. 5,974,579 to Lepejian et al. (herein "the Lepejian patent"). In response, the rejections are traversed and consideration of the following Remarks is respectfully requested.

Claim 26 is rejected as anticipated by the Lepejian patent. Specifically, the Office Action notes that the "transition and capacitively coupled faults" as taught in the Lepejian patent are equivalent to the faults caused by stimulation of non-deterministic operations as taught in the present Specification. See May 18, 2005 Office Action page 3, lines 12-16. In response, claim 26 remains unamended and the rejection is respectfully traversed. An anticipation rejection is proper only when all elements and limitations that are recited in the rejected claim are found in the prior art. The Lepejian patent does not disclose "a decoder accepting the test codes and remapping each test code to at least two test enable signals wherein the test enable signals logically combine with the control lines to stimulate only deterministic operations when in a test enabled condition". The Specification defines non-deterministic operations to be "contention conditions that would not occur during actual operation of the IC". See page 2, lines 9-10 and page 6, lines 15-26 of the present

Specification. As an example, a deterministic operation is a memory read/read operation from the same memory location and a nondeterministic operation is a write/write to the same memory location. It is stimulation of the nondeterministic operations during a built in self-test ("BIST") that are avoided in the apparatus of claim 26. By contrast, "transition and capacitively coupled faults" as taught in the Lepejian patent are actual faults inherent in the tested product that are found by testing deterministic operations at full speed and detecting a test failure. See col. 3, lines 53-58 of the Lepejian patent. The operations that test the "transition and capacitively coupled faults" are not avoided in the Lepejian patent because to do so would not perform the stated advantage of detecting the faults. See col. 3, lines 58-61 of the Lepejian patent. Accordingly, the "non-deterministic operations" as taught in the present Specification are not equivalent to the "transition and capacitively coupled faults" that occur during deterministic operations as taught in the Lepejian patent. The teachings of the Lepejian patent disclose testing only deterministic operations, but within a limited valid address space and does not distinguish between testing deterministic and nondeterministic operations of the memory as recited in claim 26.

The May 18, 2005 Office Action further proposes that the Lepejian patent shows a decoder (85) accepting test codes (12) and remaps the test codes

(12) to test enable signals (86). The Office Action further proposes that de-skewing circuit (FIGURE 4) logically combines the test enable signals (86) with control lines (mode control 11) to stimulate only deterministic operations when in a test enabled condition. See May 18, 2005 Office Action page 4, lines 1-11. From a review of FIGURE 4 of the Lepejian patent, however, the mode control (11) are not logically combined with any signals coming from the decoder (85). It appears that the de-skewing circuit (70) halts the clocking of address lines (51) in the presence of a low address halt signal (52), but permits propagation of the mode control (11) as clocked by the sync clock (19) regardless of the address halt signal (52) status. Accordingly, the Lepejian patent does not disclose all elements and limitations of Claim 26, and therefore, cannot anticipate the claim. For these and other reasons, withdrawal of the rejection of claim 26 is respectfully requested.

Claims 2-6 and 27-30 are rejected as anticipated by the Lepejian patent. Claims 2-6 remain unamended. Claims 2-6 depend from claim 26, which is believed to be allowable. Accordingly, Claims 2-6 are believed to be allowable for at least the same reasons claim 26 is believed to be allowable and withdrawal of the rejection of claims 2-6 is respectfully requested.

Claim 31 is rejected as anticipated by the Lepejian patent. In response, claim 31 is amended to remove the "repeatably" limitation and the

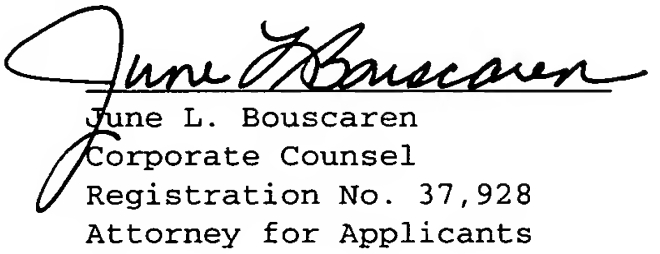
rejection is respectfully traversed. In order for the Lepejian patent to properly anticipate a claim, each and every element and their limitations must be found in the prior art. The Lepejian patent does not suggest or disclose the steps of "remapping the test codes to at least two test enable signals" and then "logically combining the test enable signals with the control lines to stimulate only the deterministic operations when in a test enabled condition". FIGURE 4 of the Lepejian patent does not show a logical combination of any lines from the decoder (85) with the mode control (11), but shows pass through of the mode control (11) to the control signal (83) via the synch clock (19). The control signal (83) is returned and is not used for stimulating operations in the memory under test when in a test enable condition. Because this logical combining step is not present in the Lepejian patent, then the Lepejian patent does not show all elements and limitations for claim 31 and, therefore, does not properly anticipate the method of claim 31. Accordingly, withdrawal of the rejection of claim 31 is respectfully requested and allowance is solicited.

Claims 8-12 and 32 are rejected as anticipated by the Lepejian patent. Claims 8-12 depend from claim 31 and are believed to be allowable for at least the same reasons claim 31 is believed to be allowable. Withdrawal of the rejection of claims 8-12 and 32 is respectfully requested.

If any clarifications can be made by way of telephonic interview, the Examiner is invited to contact the Undersigned.

Respectfully submitted,

Stong et al.
Applicant(s)



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